Name:	
Enrolment No:	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, May/June 2022

Program Name: B.Tech (CSE-All Courses)
Semester: II
Course Name : Computer System Architecture **Time : 03 hrs.**
Course Code : CSEG1014 **Max. Marks: 100**
Nos. of page(s) : 03
Instructions: Answer the following questions.

SECTION A

S. No.		Marks	CO
Q1	The program below uses six temporary variables a, b, c, d, e, f. a = 1 b = 10 c = 20 d = a+b e = c+d f = c+e b = c+e e = b+f d = 5+e return d+f Assuming that all operations take their operands from registers, what is the minimum number of registers needed to execute this program without spilling?	4	CO1
Q2	Consider the following min term expression of F: $F(P,Q,R,S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$ The minterms 2, 7, 8 and 13 are "do not care" terms. Find the minimal sum-of-product form for F.	4	CO2
Q3	A) Convert the hexadecimal number F3A7C2 to binary and octal. B) Convert the following binary number to decimal:1011110,1110101 C) Find the 9's compliment of following eight digit decimal number: 12349876 , 00980100	4	CO2
Q4	Describe the role of control unit during instruction execution.	4	CO3
Q5	Enumerate the advantages and disadvantages of direct and full associative mapping between cache and main memory.	4	CO4

SECTION B

Q6	Explain Instruction cycle in detail. Differentiate between Branch Unconditionally (BUN) and Branch and Save Return Address (BSA) memory reference Instructions	(6+4)	CO1
Q7	Differentiate between Hardwired and microprogrammed control unit. Define the following (a) micro operation (b) microinstruction (c) microprogram (d) microcode	(6+4)	CO3
Q8	Define Priority Interrupt. Explain sequential hardware method of solving the Priority Interrupt with the help of suitable diagram.	(4+6)	CO4

Q9	A computer uses RAM chips of 1024x1 capacity. Calculate: **i)** How many chips are needed and how should their address line be connected to provide memory capacity of 1024 bytes. **ii)** How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. **OR** Explain the concept of memory hierarchy and why do we have different types of memory in a computer system?	**(5+5)**	**CO4**
	SECTION-C		
Q10	**A)** Explain in detail the process of DMA transfer with the help of suitable diagrams. State clearly the meaning of cycle stealing. **B)** An instruction is stored at location 300 with its address field at location 301.The address field has value 400.A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative **OR** **A)** Enumerate and differentiate between different types of interrupts. Explain interrupt cycle in detail**.** **B)** Suppose we have the instruction Load 1000. Given memory and register R1 contain the values below: Memory 1000 1400 ... 1100 400 ... 1200 1000 ... 1300 1100 ... 1400 1300 R1 200 Assuming register R2 has content as 1300, determine the actual value loaded into the accumulator. Show the appropriate calculation wherever needed: i) Immediate ii) Direct iii) Indirect iv) Indexed with R1 as Index register v) Register indirect taking R2 in consideration	**(5+5)** **(3+3+4)** **(5+5)** **(2x 5)**	**CO4, CO1**
Q11.	**A)** Write a sequence of assembly level instructions that will compute the value of {x =(A +B) * (C + D)} using (i) Three-address instructions (ii) Two-address instructions (iii) One-address instructions **B)** A digital computer has a memory unit of (64K X 16) and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words. (i) How many bits are there in the tag, index, block, and word fields of the address	**(3+3+4)** **(4+3+3)**	**CO 2,CO 4**

	format? (ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. (iii) How many blocks can the cache accommodate?		