UPES

UPES
End Semester Examination, December 2023

Course: Digital Electronics   Semester: I
Program: BSC (CS)   Time: 03 hrs.
Course Code: ECEG 1010   Max. Marks: 100
Instructions: Attempt all the questions

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	What do you understand by Universal gates? Design and Implement Ex-OR and AND gates using NAND gate.	4	CO1
Q 2	Differentiate the following (a) Decoder and Demultiplexer (b) Combinational and Sequential circuits	4	CO1
Q 3	Simplify the Boolean expression using K-map $F(A, B, C, D) = \sum(1, 2, 4, 5, 6, 8, 9, 12)$	4	CO2
Q 4	Design and implement Full Adder with its truth table and logic diagram.	4	CO3
Q 5	Convert the following: (a) $(348.65)_{10}$ to hexadecimal (b) $(461.47)_8$ to decimal	4	CO4

SECTION B
(4Qx10M= 40 Marks)

Q 6	What do you understand by registers? Discuss with suitable logic diagram all the four configuration SISO, SIPO, PISO, PIPO of registers.	10	CO5
Q 7	Simplify the expression $F(A, B, C, D) = M (1, 3, 5, 8, 9, 11, 14)$ +d (2, 7, 10) using K-map and implement the result using logic gates.	10	CO2
Q 8	Derive an expression for any two seven segments using BCD to 7-segment decoding technique and draw its diagram and K-map.	10	CO3
Q 9	Design and implement T flip-flop using S-R flip-flop with excitation table.	10	CO4

SECTION-C
(2Qx20M=40 Marks)

Q 10	(a) Explain the function of multiplexer with its detailed diagram and implement the following function using 8×1 Multiplexer $F (A, B, C, D) = \Sigma (1, 3, 4, 7, 9, 11, 13, 15)$	20	CO1

	(b) Discuss the following codes in detail
	   i. Error detecting codes
	   ii. Error correcting or Hamming codes
	   iii. Weighted binary codes
	   iv. Non-weighted codes
	   v. Alphanumeric codes		

Q 11	(a) Classify flip-flops in detail and design a J-K flip flop using NAND gates with its truth table, state diagram, excitation table and implement the expression for next state output with the help of K-map. (b) Design a master-slave J-K flip flop and verify the race-around condition.	**20**	**CO4**