Name: **Enrolment No:**	

UPES

End Semester Examination, May 2024

Course: Digital Electronics **Semester: II**

Program: B.Tech Computer Science

Time : 03 hrs.

Course Code: ECEG1012 **Max. Marks: 100**

Instructions: Scientific Calculators are not allowed.

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Design a two input NAND gate with CMOS logic.	**4**	**CO1**
Q 2	Perform the following BCD arithmetic: (a) 24 – 68 (b) 00011001 + 00010100	**4**	**CO1**
Q 3	Define analog to digital converter. What are their applications?	**4**	**CO3**
Q 4	Convert JK Flip-Flop to T Flip-Flop.	**4**	**CO2**
Q 5	Illustrate with example different types of flags in 8085 microprocessor.	**4**	**CO4**

SECTION B
(4Qx10M= 40 Marks)

Q 6	Using the K-map method simplify the following Boolean function in SOP form. $Y = \sum_m (0,2,3,6,7) + \sum_d (8,10,11,15)$	**10**	**CO2**
Q 7	Explain the operation of the following shift registers: (a) Serial Input Serial Output Shift Register (SISO) (b) Parallel Input Serial Output Shift Register (PISO)	**10**	**CO2**
Q 8	Design a 4-bit Asynchronous UP Counter.	**10**	**CO2**
Q 9	Describe the principle of operation of any type of A/D converter using a suitable diagram. OR Describe the principle of operation of any type of D/A converter using a suitable diagram.	**10**	**CO3**

SECTION-C
(2Qx20M=40 Marks)

Q 10	(a) Describe the pin diagram of 8085 along with the description of each pin. (b) Draw the timing diagram of the following instruction: 2000 MVI A, 32H.	**10** **10**	**CO4**
Q 11	(a) Design 3-bit UP/DOWN Synchronous Counter using D Flip-Flops. (b) Design a sequence generator with the following sequence: 0-2-4-5-1-7-6 using suitable flip-flops. OR (a) Design a MOD-6 synchronous counter using JK Flip-Flops. If during counting, the sequence goes to any unused state, it should come back to any used state . (b) Design a sequence generator using D Flip-Flop to generate the sequence 101100110.	**10** **10** **10** **10**	**CO2**